What is claimed is:

1. A method of delivering a command in a bus system including one or more master devices and two or more slave devices, the method comprising the steps of:

(a) delivering a first command to a first slave device; and

(b) delivering a second command to a second slave device at a point in time which is less than or equal to a latency time of the second slave device in advance of the completion of data transfer according to the first command.

2. The method of claim 1, prior to the step (b), further comprising the steps of:

(b1) the first slave device informing a corresponding master device of pseudo execution completion indicating that data transfer is complete at a point in time which is less than or equal to the latency time of the second slave device in advance of the completion of data transfer according to the first command; and

(b2) receiving the second command for the second slave device upon receipt of the pseudo execution completion information.

3. The method of claim 1, wherein the first and second slave devices each include a memory device and a slave controller for controlling the memory device,

wherein the step (a) comprises the step of delivering the first command to a first slave controller, and

wherein the step (b) comprises the step of (b′) delivering the second command to a second slave controller at a point in time which is less than or equal to the latency time of the second slave device in advance of the completion of data transfer according to the first command.

4. The method of claim 3, prior to the step (b′), further comprising the steps of:

(b′1) the first slave controller informing a corresponding master device of pseudo execution completion indicating that data transfer is complete at a point in time which is less than or equal to the latency time of the second slave device in advance of the completion of data transfer according to the first command; and

(b′2) receiving the second command for the second slave device from the corresponding master device that has received the pseudo execution completion information.

5. The method of claim 3, wherein each memory device is a synchronous dynamic random access memory (SDRAM), and the slave controller is an SDRAM controller.

6. A method of delivering a command in a bus system including a master device and two or more slave devices, at least one of the slave devices having a latency time for data input/output, the method comprising the steps of:

(a) providing respective difference values between a longest of the latency times of all the slave devices and the latency time of each slave device;

(b) receiving a first command for a first slave device from the master device; and

(c) delivering the first command to the first slave device after a time equivalent to the difference value corresponding to the first slave device has lapsed.

7. The method of claim 6, further comprising the step of (d) delivering a second command to a second slave device at a point in time which is less than or equal to a latency time of the second slave device in advance of the completion of data transfer according to the first command.

8. A bus system including a master device and two or more slave devices, at least one of which has a latency time for data input/output, the bus system comprising a pseudo-delayer for delivering a second command to a second slave device at a first point in time which is less than or equal to a latency time of the second slave device in advance of a second point in time when a first slave device completes data transfer according to a first command.

9. The bus system of claim 8, wherein the first slave device informs a corresponding master device of pseudo execution completion information at a third point in time which is less than or equal to a latency time of the second slave device in advance of the completion of data transfer according to the first command, and the corresponding master device receiving the pseudo execution completion information delivers the second command to the pseudo-delayer.

10. The bus system of claim 8, wherein the first and second slave devices each comprise a memory device, and a slave controller for controlling the memory device, and

wherein the pseudo-delayer delivers the first command to a first slave controller, and delivers the second command to a second slave controller at a fourth point in time which is less than or equal to the latency time of the second slave device in advance of the completion of data transfer according to the first command.

11. The bus system of claim 10, wherein the first slave controller informs a corresponding master device of a pseudo execution completion at a fifth point in time which is less than or equal to the latency time of the second slave device in advance of the completion of data transfer according to the first command, and

wherein the corresponding master device delivers the second command to the pseudo-delayer upon receipt of the pseudo execution completion.

12. The bus system of claim 10, wherein each memory device is a synchronous dynamic random access memory (SDRAM), and the slave controller is an SDRAM controller.

13. A bus system including a master device and two or more slave devices, at least one of which has a latency time for data input/output, the bus system comprising a pseudo-delayer which includes a storing unit for storing a number of delay clock cycles which corresponds to respective differences between a longest of the latency times of all the slave

devices and the latency time of each slave device, which receives a first command for a first slave device from the master device, and which delivers the first command to the first slave device after a number of delay clock cycles corresponding to the number stored in the storing unit for the first slave device have lapsed.

14. The bus system of claim 13, wherein the first slave device includes a memory device and a slave controller for controlling the memory device,

wherein the slave controller informs a corresponding master device of pseudo execution completion at a point in time which is the longest of the latency times in advance of the completion of data transfer according to the first command, and

wherein the corresponding master device delivers the second command to the pseudo-delayer upon receipt of the pseudo execution completion information.